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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/845,405	04/30/2001	Gerhard Beitel	GR 00 P 4091	2869

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EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 12/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/845,405	BEITEL ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-12* is/are allowed.

6)☒ Claim(s) *1 and 4-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/845,405* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/19/2003 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1, 4, 5, 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Buskirk et al (US 6,346,741)

Van Buskirk discloses a method for forming an integrated circuit. This method comprises the steps of:

providing a substrate (fig. 1D)

forming the structured electrode layers 30 and 34 of a noble metal (Pt) on the substrate, (col 14, lines 9-17), the structured layers 30 and 34 are to be removed in a polishing step (fig. 1E), fig. 1D of Van Buskirk shows that the structured electrode layers 30 and 34 having the width of greater than twice the thickness of the layers, which reads on forming the structures on the substrate with an aspect ratio of greater than 2

forming/depositing an dielectric layer 35 (silicon oxide) on the structured layers 30, 34 and the substrate (col 13, lines 55-56, col 14, lines 9-11 ; fig. 1D), the dielectric layer 35 is removed in a polishing step (fig. 1E), which reads on depositing a sacrificial layer on the structure to be removed and the substrate

performing a CMP process to planarize and remove the structured layers 30, 34/structures to be removed and the dielectric layer 35/sacrificial layer (col 14, lines 48-50, fig. 1E)

The limitations of claims 4, 5 have been discussed above

Regarding claim 7, fig. 1D of Van Buskirk also shows that the structured electrode layers 30 and 34 having a width much greater than the thickness of the layers, which reads on forming the structures on the substrate with an aspect ratio of greater than 4

4. Claims 1, 4, 5, 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Choi (US 6,030,866)

Choi discloses a method for manufacturing a capacitor. This method comprises the steps of:

providing a substrate (fig. 3D)

forming the structured electrode layers 67 of a noble metal (Pd) on the substrate, (col 4, lines 46-48), the structured layers 67 are removed in a polishing step (fig. 3E), fig. 3D of Choi shows that the structured electrode layers 67 having the width of greater than twice the thickness of the layers, which reads on forming the structures on the substrate with an aspect ratio of greater than 2

forming/depositing an dielectric layer 69 (silicon oxide) on the structured layers 67 and the substrate (col 4, lines 54-55 ; fig. 3D), the dielectric layer 69 is removed in a polishing step (fig. 3E), which reads on depositing a sacrificial layer on the structure to be removed and the substrate

performing a CMP process to polish and remove the structured layers 67/structures to be removed and the dielectric layer 69/sacrificial layer (col 4, lines 56-58, fig. 3E)

The limitations of claims 4, 5 have been discussed above

Regarding claim 7, fig. 3D of Choi also shows that the structured electrode layers 30 and 34 having a width much greater than the thickness of the layers, which reads on forming the structures on the substrate with an aspect ratio of greater than 4

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Buskirk et al (US 6,346,741) in view of Ismail et al (US 5,955,759)

Zurcher's method has been described above in paragraph 3. Unlike the instant claimed inventions as per claim 6, Van Buskirk fails to disclose the step of removing residue of the sacrificial layer by wet processes followed the CMP.

However, Ismail discloses a method for manufacturing a semiconductor device using CMP comprises the step of removing the remaining sacrificial layer 1 by wet etching (col 3, line 48-49)

Hence, one skilled in the art would have found it obvious to modify Van Buskirk's method by adding the step of removing the remaining sacrificial layer 1 by wet etching as per Ismail after the CMP step because Ismail teaches that sacrificial layer is preferably removed by wet etching to avoid reactive ion etching damage to the semiconductor structure (col 3, lines 49-50)

Allowable Subject Matter

7. Claims 8-12 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claim 8, the cited prior arts of record fail to disclose the step of performing a polishing step to remove the redepositions of the layer (redeposition that emerge at the sidewalls of the mask) being structured so that a structured layer emerges. Since the closest cited prior art of Chien et al (US 5,702,869) discloses that all

the surrounding (conductive interconnection stud) of Chien's redepositions 27a on the sidewall of a mask 26a are of fundamental importance to Chien device's operativeness, thus performing a polishing step to remove the redepositions in Chien would have removed the surrounding of Chien's redeposition and rendered Chien' s device inoperable.

Response to Arguments

8. Applicant's arguments with respect to claims 1, 4-7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 703 305-2667. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

LV
December 4, 2003